Using Intersil Digitally Controlled Potentiometers in Commercial RF Power Amplifier Applications

Application Note | May 5, 2005 | AN136.0

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Introduction

In the past, design techniques for setting bias conditions on RF power amplifiers required the use of either an unreliable mechanical potentiometer or a "hammer-and-nut" solution using a (typically 8-bit) DAC. The former is extremely unreliable, and often makes nonsense of reliability and MTBF calculations. The latter approach is relatively expensive, since the designer will make little or no use of the DAC performance capabilities that they are paying top dollar for.

An innovative new technique has emerged. Using a element called a XDCP (Intersil digital controlled potentiometer), designers can radically improve the cost and reliability of RF power amplifiers. This is particularly valuable in demanding applications such as cellular basestations using high linearity and high efficiency LDMOS technology.

The XDCP is ideally suited for this application, and exceeds the reliability, programmability and cost specifications of this requirement completely.

The new generation XDCP contains no charge pumps, and therefore no external noise is introduced onto the wiper, even when programming. It is possible therefore, to dynamically reprogram the XDCP and still maintain CW (continuous wave) power on the amplifier (the wiper resistance executes a smooth transition between the old and new states). This is an important issue for rebiasing amplifiers that share different modulation standards, which consequently may require different operating points for optimum performance.

XDCPs have established millions of problem-free field hours in commercial power amplifiers (PA) installed in communication networks all over the world.

Power Amplifier Overview—Architectures & Applications

Power amplifier specification involves the selection of several key parameters. These are a combination of output power, efficiency, linearity and bandwidth. Consideration of these parameters will generally dictate the class of operation (biasing conditions) and choice of technology for the amplifier.

The class of operation, Figure 1, specifies the conduction angle of the MOS amplifier (the portion of the input signal which is amplified), and is set by the gate voltage.

FIGURE 1.

CLASS	CONDUCTION ANGLE (Θ)	THEORETICAL MAXIMUM EFFICIENCY
A	360	50
AB	$180 < \theta < 360$	50–78.5
B	180	78.5
C	$\theta < 180$	>78.5

Other classes of operation are also possible, although the spectrum of available efficiencies is adequately illustrated with the above examples. It is fundamentally important to understand however, that linearity and efficiency are inversely proportional!

The choice of circuit technology is an evolving one. Certainly, below 2.5GHz and above 1W output power, LDMOS rules the roost. GaAs (Gallium Arsenide) and bipolar technologies are also popular for this combination of power and frequency, but can not match the superior salient characteristics of LDMOS. As a matter of fact, an LDMOS transistor biased class AB will give a better linearity/efficiency characteristic than both GaAs and bipolar formats even when the latter are biased class A (which is supposed to be the most linear of all classes!).

Amplifier architecture is the next important consideration. Generally, the choice will be dictated by the amplifier specification. There are three popular options; *single ended, balanced and push-pull*. The simplest of these is the single ended amplifier.

Single ended amplifiers consist of a single high power transistor, and are unpopular as they present the greatest design challenge, and as stand alone amplifiers have the greatest susceptibility to reverse intermodulation. It is generally difficult to design a high power amplifier that has good VSWR while simultaneously achieving the required output power, efficiency and linearity. Poor VSWR will, at best, cause degraded or non-optimum performance from an amplifier chain. In the worst case, out-of-band uncontrolled VSWR will cause oscillations.

To their credit however, architectures using *single ended* amplifiers usually represent the best solution in terms of PCB real estate and power transistor costs (normally measured in cost per watt). For example, a 60W amplifier constructed from a single 60W transistor will occupy less than one half of the real estate of an amplifier using 2 x 30W transistors operating balanced or push-pull. The component costs to generate a unit of power will be lower for the single ended case also.

Applications with stringent space and cost constraints will dictate the use of single ended amplifiers.

The next architecture to consider is the *balanced amplifier*, which uses two transistors operating with a conduction angle offset between them of 90 degrees. There are several advantages to using this option.

The most important is the isolation that the 3dB 90 degree hybrid offers from (and to!) the RF subsystems both upstream and downstream. Common mode reflections caused by poor VSWR from the transistor and it's matching network, are transferred to the isolated port where they are terminated. Therefore, the amount of reflected power that can cause integration problems, from the input and output ports is greatly reduced.

Additionally, the overall output power requirement is shared between two transistors. This is desirable from a thermal management point of view, as the waste heat generated can be spread across a larger area.

Of course, the number of transistors operated in a balanced amplifier configuration may be more than two. In fact, using a network of 3dB 90degree hybrids, it is possible to balance 2n transistors. This is a common method of achieving high output power levels without using large transistors while improving the degree of redundancy (a certain degree of operation if one transistor fails).

The illustration in Figure 2 shows a (3dB 90 degree) splitter hybrid at the input, two gain blocks, and a combiner hybrid at the output. Normally, diagonally opposite ports are terminated with the system impedance.

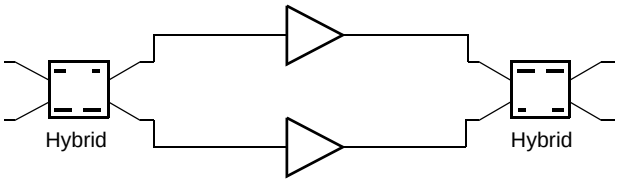

FIGURE 2.

In applications where it is possible to trade off intermodulation performance for redundancy, independent signals may be applied to each port. Amplification of the signals will be undertaken in both amplifiers, before "recombining" in the output hybrid separates the signals into the original constituents.

The balanced amplifier is normally used in multistage amplifiers, or in other applications where it is important to present low VSWR to adjacent stages in order to prevent the problems noted above. Additionally, it offers improved isolation against reverse intermodulation distortion over the single ended option.

The last conventional architecture is the *push-pull amplifier.* Again, using two transistors, but operated 180 degrees offset in their conduction angle. Traditionally, this was used in high efficiency, high power applications—normally constant envelope FM transmission.

The main advantages of the push-pull configuration are the even harmonic rejection, and the ease with which large impedance transformations can be made, as the balun transformer typically steps the impedance level down. As with the balanced amplifier, two transistors are sharing the workload between them, and therefore the job of thermal management is made somewhat easier.

Popularity of this architecture is on the increase with the recent introduction of surface mount balun transformers (well suited to automated production methods), although traditionally this was not the case for commercial applications as the balun was realized with lengths of hand soldered coaxial cable, Figure 3, greatly increasing production labor costs.

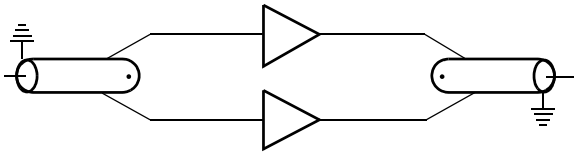

FIGURE 3.

The push-pull architecture is normally used in high efficiency (constant envelope) applications, for example FM transmission, in order to improve harmonic performance. Again, it offers improved isolation against reverse intermodulation distortion over the single ended option.

Biasing Issues

One of the most important aspects of power amplifier (PA) design is the biasing network. It is important for the bias network to reject RF power. Using high impedance sources where possible accomplishes this. Where low impedance sources are used, it is imperative to maintain a good decoupling regime, to maximize the transistor's performance.

At the FET drain (GaAs or LDMOS), it is necessary to use a low impedance bias supply. For transistors not biased class A, the current versus output power characteristic is dynamic, and any residual power supply impedance will cause amplitude modulation of the drain voltage.

Most commercial power amplifiers have a bandwidth typically of a maximum 10%, and therefore it is possible to supply drain current using a RF shorted quarter wave section (which will transform to an open circuit at the feed point). For wideband applications (octave plus), it is generally better to use a lumped inductor to feed bias to the drain.

The bias voltage may be fed onto the transistor gate matching network via a surface mount resistor. Typically, the resistance would be of the order of a few hundred ohms to ensure that minimal RF power leaks through the resistor into the biasing network. As the gate is extremely high impedance and therefore the current requirement is negligible, it is possible to use the smallest package size readily available (typically 0603). This will reduce the effect of any package parasitic resonance, maximizing stability and performance.

For LDMOS applications, thermal compensation would be done using either a simple analog compensation scheme or using DSP to control the XDCP. The gate voltage change with respect to temperature (for constant drain current) is around -2mV/°K[1]. Normally, the compensation constant would be a slightly different to this to maintain a constant gain versus temperature response.

The biasing (quiescent current) requirement varies between applications, but for a typical SCPA (single carrier power amplifier) a quiescent current tuning resolution of 1% of Idq_opt is all that is needed. This is easily achieved using an 8-bit XDCP, X9258T or X9250T with 256 wiper positions.

APPLICATION	RESOLUTION
MCPA (Multi Carrier Amplifier)	8-bit or 2 x 6-bit
Large Dynamic Conduction Angle Variation	2 x 6-bit
SCPA (Single Carrier Amplifier)	6-bit or 8-bit

1. Idq_opt is the typical bias condition, which offers maximum dynamic gain flatness and almost optimum two-tone third order intermodulation distortion when a device is biased class AB.

Some applications, for example MCPA (multicarrier power amplifier) may require finer bias control or greater dynamic range to optimize dynamic gain flatness. In some cases, it may be desirable to actually change the bias class (conduction angle) completely, from A through AB to B and possibly beyond.

This can also be easily achieved, Figure 4, using 2 XDCPs and a weighted summing network at the op-amp input… effectively doubling the bit resolution. 2 combined 6-bit (64 positions) XDCPs can achieve 12-bit (4096 positions) resolution.

By selecting the ratio R1/R2 to be the same as the number of tap points (in this case 6-bits = 64 positions), it is possible to achieve a dividing resolution of more than 4000 wiper positions. This arrangement is more than adequate to provide high resolution biasing of LDMOS devices, while giving maximum flexibility to bias the transistor in any class of operation.

The X9250 8-bit potentiometer will generally give the required voltage resolution, especially when the range of voltage outputs is conditioned. This can be done by selecting upper and lower limits for the high and low side of the potentiometer. Additionally, the op-amp buffer allows further flexibility for range adjustment and the introduction of an offset.

A typical LDMOS transistor requires a change of approximately 2.5mV in gate voltage to effect to 1% change in drain current. It is therefore possible to use a single 8-bit potentiometer to tune over a range of 0.6V with 1% resolution. Using the 2 x 6-bit potentiometer example highlighted earlier, gives the potential for 1% resolution over a 10V range, though normally the range would be reduced to allow greater resolution.

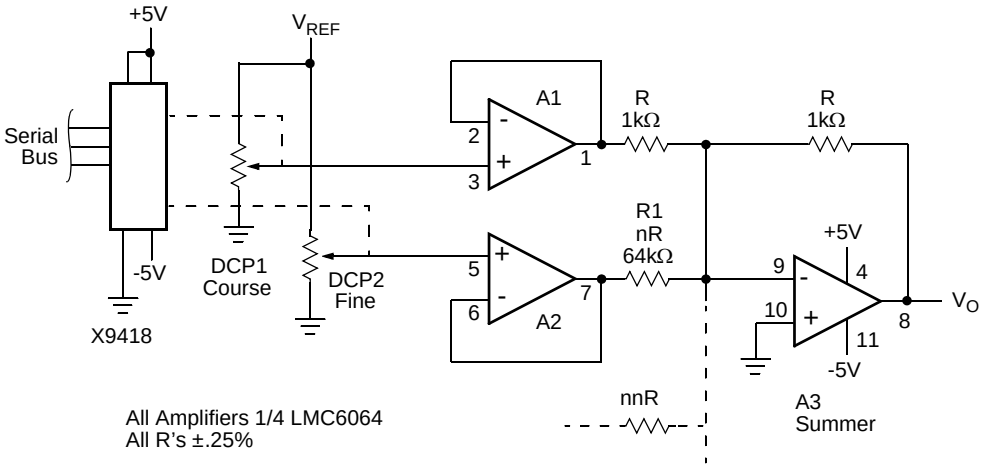

FIGURE 4.

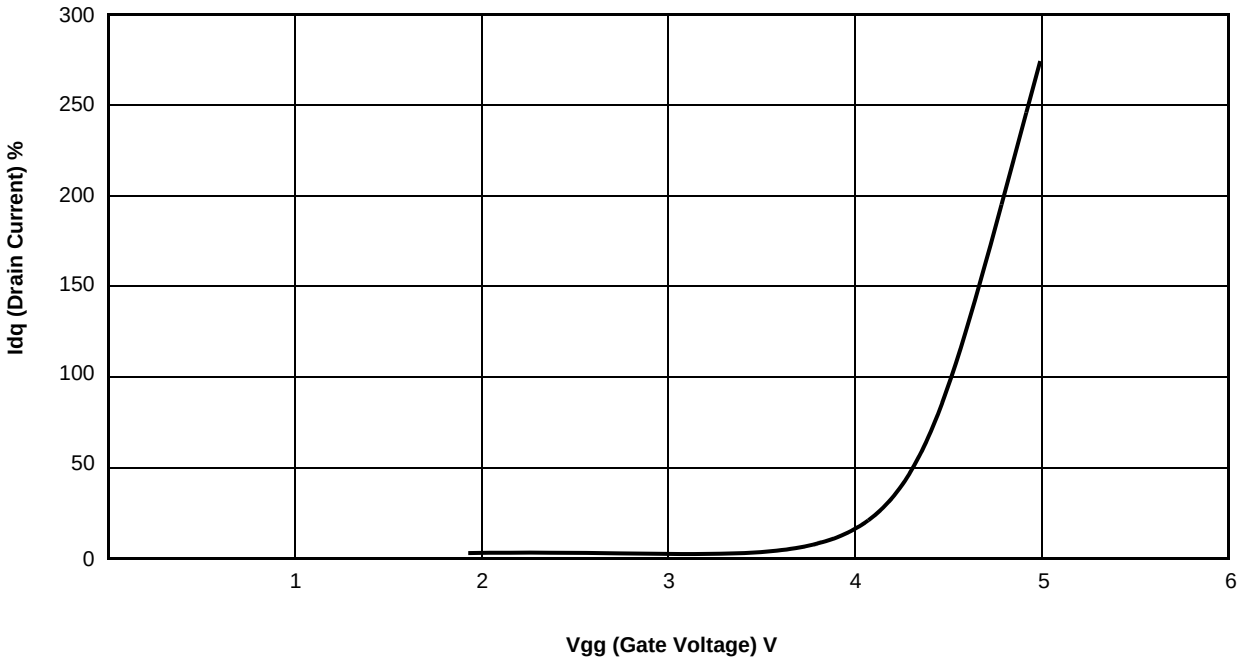

FIGURE 5.

On-chip memory is another feature incorporated in most of the XDCP range. This allows the designer to load a set of four values for each potentiometer, and dynamically assign the memory register to the potentiometer at any point in time.

Generally, it is not necessary to use these memory settings. The settings would normally be stored and controlled by an external processor and memory. Reloading new values to the wiper register doesn't result in any spurious noise at the wiper. *This allows the PA bias setting to be dynamically reprogrammed while "hot" with RF power, with no detrimental (or even detectable) effect*.

This is theoretically the worst time possible to change bias conditions on the transistor, as any spikes on the bias supply could result in large amounts of current drawn by the transistor, enhanced by the RF power, with possibly terminal consequences.

The memory settings are most likely to be utilized for many power amplifier design features

- Digital thermal compensation
  - Thermal conditions are monitored by the system microcontroller. The controller can use a look-up table or algorithm to calculate the best operating point for the transistor. A preset list of discrete values can be loaded into the memory at production time, and loaded into the wiper register when necessary.
- Vg/Id drift compensation
  - LDMOS transistors suffer from performance drift, Figure 6, over time. The net effect is that a slightly increased amount of gate voltage is required to maintain a given drain current. LDMOS processes are being refined continually, and current drift figures are typically 5% over 20 years. Most of this drift occurs while the amplifier is undergoing test in the factory; effectively burning the device in, before delivery. Drift is also proportional to the process cut-off frequency.

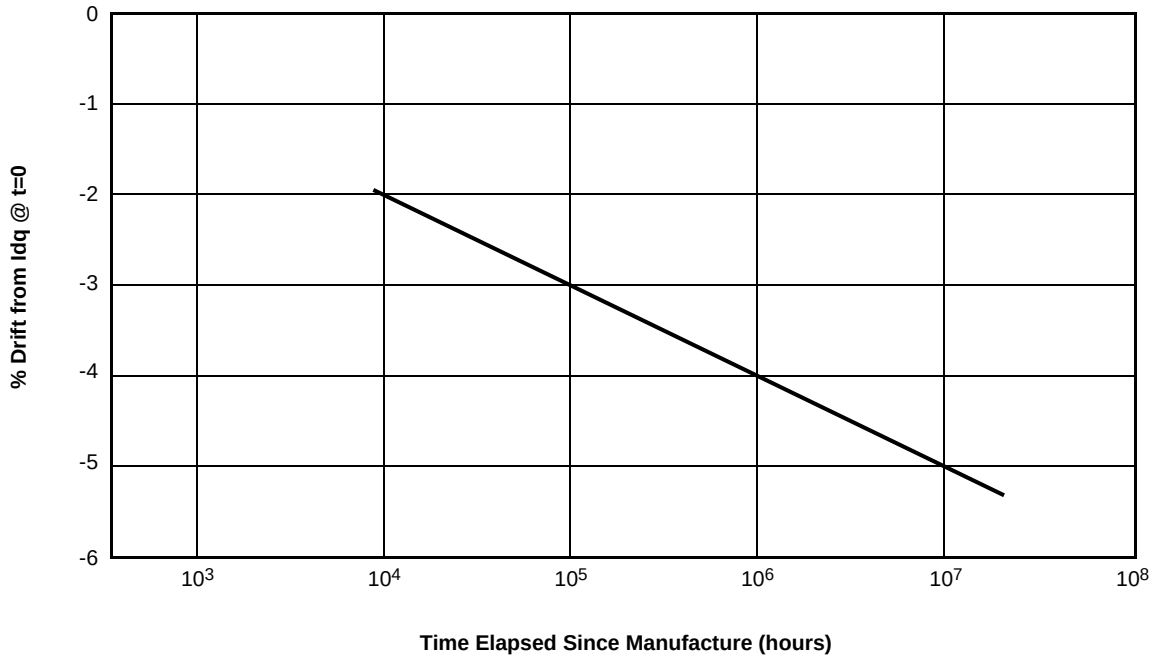

FIGURE 6.

PCB Layout/Configuration & Production Interface

PCB layout – source from Intersil

Other RF Applications – An Example

The XDCP can be used in a wide variety of other RF applications. A good example would be the vector modulator. The purpose of the vector modulator is to manipulate an arbitrary signal, allowing it's amplitude and phase to be varied in a controlled manner. Recently, it has become a popular method for complex gain adjustment in linearized amplifier systems, both feedforward and predistortion.

The vector modulator consists of a 3dB 90degree hybrid, an in-phase combiner, and 2 variable attenuators, realized either with a pair of mixers or 2 further 3dB 90 degree hybrids with diodes. Analysis of the vector modulator is straightforward, and is not detailed here.

The advantages of using a XDCP over a DAC are the same as for the power amplifier application. The vector modulator example serves only to highlight another of the numerous applications where significant benefit can be derived.

Summary

The XDCP offers the reliability and flexibility of the DAC for the cost of the mechanical potentiometer, giving the designer the rare opportunity to make a win-win design improvement.

The new software interface allows easy prototyping of a dynamic programming environment with a minimum of hardware.

Flexibility of the XDCP is such that it may also be used in the PA periphery and control circuitry, not only for biasing of transistors. Additionally, it may supersede the use of the DAC in other cost critical RF subsystems.

Glossary

XDCP - Intersil Digital Controlled Potentiometer; a component that obsoletes mechanical potentiometers and enhances dynamic circuit control.

DAC - Digital to Analog Converter; generates an output voltage proportional to a digital word.

LDMOS - Laterally Diffused MOS; A relatively new semiconductor technology in the commercial RF Power market. Has much better operating characteristics than bipolar and other FET technologies, and is generally the first choice technology in power amplifier applications up to 2.5GHz.

CW - Continuous Wave; used to describe a signal operating at a constant power/envelope (such as FM radio transmission), similarly used to describe an amplifiers ability to handle a continuous high power signal.

PEP - Peak Envelope Power; a PEP signal a signal envelope whose amplitude changes with time, and is usually described by a peak to mean ratio.

VSWR - Voltage Standing Wave Ratio; When a signal is incident on a boundary/discontinuity, an amount of the signal is reflected and interferes with the incident signal to create a standing wave (the sum of two waves travelling in opposite directions).

SCPA - Single Carrier Power Amplifier; a power amplifier used to boost the signal level of a single signal (although many signals maybe transmitted through a SCPA when multiplexed in the time domain). In theory, a SCPA is less efficient and cost effective than a MCPA.

MCPA - Multi Carrier Power Amplifier; a power amplifier used to boost the level of several channels simultaneously. Intermodulation distortion is the limiting factor in the implementation of MCPA subsystems, especially for the GSM standard.

X9250T= 256 steps, Quad, SPI, Low noise/Power.

X9258T= 256 steps, Quad, IIC, Low noise/power

Gareth Lloyd was educated at The University of Leeds, UK and Pennsylvania State University, USA. He graduated with a first class bachelors degree (with honours) in Electronic & Electrical Engineering before embarking on his RF career. In 1996, he became an independent consultant specializing in the field of Power Amplifiers, and has consulted on a wide variety of projects across the EU and USA, for a range of OEMs.